

IPC/JEDEC J-STD-020B

May 2002

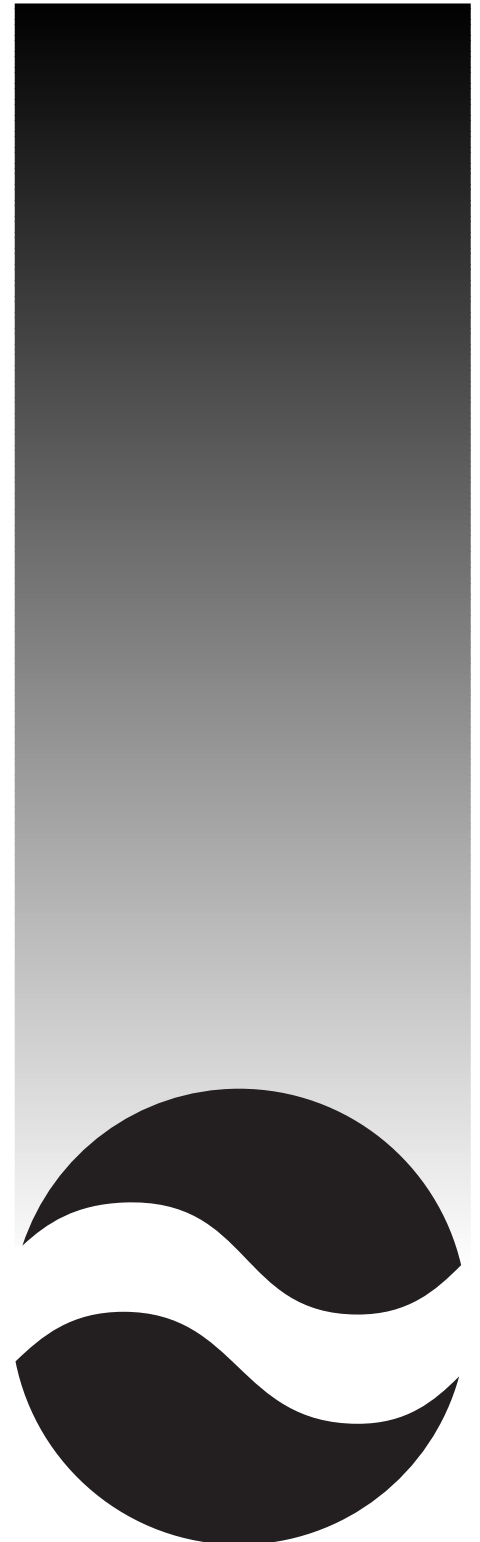
Supersedes IPC/JEDEC J-STD-020A

April 1999

JOINT INDUSTRY STANDARD

Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

Interim Final



Notice

EIA/JEDEC and IPC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of EIA/JEDEC or IPC from manufacturing or selling products not conforming to such Standards and Publications, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than EIA/JEDEC and IPC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by EIA/JEDEC and IPC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, EIA/JEDEC and IPC do not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are also wholly responsible for protecting themselves against all claims of liabilities for patent infringement.

The material in this joint standard was developed by the EIA/JEDEC JC-14.1 Committee on Reliability Test Methods for Packaged Devices and the IPC Plastic Chip Carrier Cracking Task Group (B-10a)

For Technical Information Contact:

**Electronic Industries Alliance/
JEDEC (Joint Electron Device
Engineering Council)**
2500 Wilson Boulevard
Arlington, VA 22201
Phone (703) 907-7560
Fax (703) 907-7501

IPC
2215 Sanders Road
Northbrook, IL 60062-6135
Phone (847) 509-9700
Fax (847) 509-9798

Please use the Standard Improvement Form shown at the end of this document.



ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®



IPC/JEDEC J-STD-020B

Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

A joint standard developed by the EIA/JEDEC JC-14.1 Committee on Reliability Test Methods for Packaged Devices and the B-10a Plastic Chip Carrier Cracking Task Group of IPC

Supersedes:

IPC/JEDEC J-STD-020A -
April 1999
J-STD-020 - October 1996
JEDEC JESD22-A112
IPC-SM-786A - January 1995
IPC-SM-786 - December 1990

Users of this standard are encouraged to participate in the development of future revisions.

Contact:

EIA/JEDEC
Engineering Department
2500 Wilson Boulevard
Arlington, VA 22201
Phone (703) 907-7500
Fax (703) 907-7501

IPC
2215 Sanders Road
Northbrook, IL 60062-6135
Phone (847) 509-9700
Fax (847) 509-9798

Acknowledgment

Members of the Joint IPC-EIA/JEDEC Moisture Classification Task Group have worked to develop this document. We would like to thank them for their dedication to this effort. Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the Joint Moisture Classification Working Group are shown below, it is not possible to include all of those who assisted in the evolution of this Standard. To each of them, the members of the EIA/JEDEC and IPC extend their gratitude.

IPC Packaged Electronic Components Committee

Chairman
Martin Freedman
AMP, Inc.

EIA/JEDEC JC 14.1 Committee

Chairman
Jack McCullen
Intel Corporation

EIA/JEDEC JC 14

Chairman
Nick Lycoudes
Motorola

IPC Plastic Chip Carrier Cracking Task Group, B-10a

Chairman
Steven Martell
Sonoscan, Inc.

Joint Working Group Members

Donald Abbott, Ph.D., Texas Instruments Inc.

Annalie Acosta, Tundra Semiconductor

David C. Adams, Rockwell Collins

Tim Adams, Silicon Storage Technology

Syed Sajid Ahmad, Micron Technology Inc.

Jeremy Alonte, ST Assembly Test Services

Diek Albertus, Albertus Electronics

Michael Aldrich, Analog Devices Inc.

Francis Anglade, Metronelec

Lisa Angle, Teradyne Connection Systems

Seema Apte, Electronics Regional Test Lab

Ali Asiaban, Allegro MicroSystems

Jess J. Baker, Robotic Process Systems Inc.

Jim Beal, ITT Industries

Dennis F. Bernier, Kester Northrop Grumman

Mark Bird, Amkor Technology

Gerald Leslie Bogert, Bechtel Plant Machinery, Inc.

Edwin Bradley, Ph.D., Motorola Inc.

Charles W. Bradshaw, OMG Americas

Jason Bragg, Celestica International Inc.

Peter Bratin, Ph.D., ECI Technology, Inc.

Christopher Brigham, Hi/FN

Steve Brockett, Triquint Semiconductor

Maurice Brodeur, Analog Devices

Robert V. Burress, Aguila Technologies

Jeff Cannis, Amkor Technology Inc.

Pete Cannon, Atmel

Brad Carlson, Sheldahl Inc.

Thomas A. Carroll, Boeing Space Systems

Alan S. Cash, Northrop Grumman Corporation

Srinivas Chada, Ph.D, Motorola Inc.

Tim Chaudhry, Broadcom

Sidney Cheng, OMG Americas

Sunil K. Chhabra, SUNY (State Univ. of New York)

Beverly Christian, Ph.D., Research In Motion Limited

Elaine Colokathis, Alternate Final Finishes, Inc.

David J. Corbett, Defense Supply Center Columbus

Harlan Cramer, Northrop Grumman

Donald P. Cullen, MacDermid, Inc.

Charles Dal Currier, Ambitech Inc.

Derek D'Andrade, Surface Mount Technology Centre

J. Gordon Davy, Northrop Grumman Corporation

Louis Dechiaro, Lucent Technologies

Stefan Dick, Sud-Chemie Performance Packaging

Don Dilley, ATP Electronics Inc.

Anant Dixit, Qualcomm

Mary Dinh, Northrop Grumman Space Systems

Nick D'Onofrio, CAE Electronics Ltd.

David A. Douthit, LoCan, LLC

Richard M. Edgar, Florida CirTech

Donald A. Elliott, Elliott Technologies Inc.

David Erhart, ON Semiconductor

Peter Ersland, M/A-Com

Bruce Euzent, Altera

Barry Fernelius, Agilent Technologies

John Finn, Elpida Memory

Dennis Fritz, MacDermid, Inc.

William Full, Philips Semiconductor

Alelie Funcell, Xilinx

Robert G. Farrow, Lucent Technologies Inc.

Mike Gibson, Adaptec

Izzy Gonzalez, General Semiconductor

Jean Gordon, Fairchild Semiconductor

Brian Greer, Alpha Metals

Detlef Griessman, Delphi Delco Electronics

Norman Griffin, AMD

Gerald J. Griswold, Texas Instruments Inc.

John Groom, Transmeta
William Guthrie, IBM
William B. Hampshire, Hampshire
Technical Services
Carol A. Handwerker, Sc.D., NIST
Rodney Hartbauer
Joel Heebink, Honeywell
James D. Herard, IBM Endicott
Electronics Packaging
Steven A. Herrberg, Raytheon
Systems Company
Raif Hijab, T-Ram
David D. Hillman, Rockwell Collins
Phillip E. Hinton, Hinton 'PWB'
Engineering
Andy Hirata, Sharp Microelectronics
Ronald A. Hollandsworth, ITT
Industries
Bruce Houghton, Celestica Inc.
Christopher Hunt, Ph.D., National
Physical Laboratory
Walter Jopke, PolarFab
Lesley M. Kao, Raychem CI &PP
Prakash Kapadia, Celestica
International Inc.
Mario Kasilag, Northrop Grumman
Space Systems
Mark Kelsey, Aspen Research
Corporation
Soo Hyung Kim, Samsung
Electronics
Gregg Klawson, General Dynamics -
C4 Systems
Robert Knoell, Visteon
Tom Kole, Sirenza Microdevices
Jeffry F. Koon, Raytheon Company
Connie M. Korth, Reptron
Manufacturing Services/Hibbing
Mark A. Kwoka, Intersil Corporation
David Lai, Siliconware USA
Leo P. Lambert, EPTAC Corporation
John W. Lampe
Leo LeBlanc, EMC
Frederic W. Lee, Northrop Grumman
Norden Systems
Kuan-Shaur Lei, Compaq Computer
Corporation
David W. LeMay, Silicon Graphics
Computer System
Chou H. Li, LMI Technologies
Boen Li, Photocircuits Corporation
Scott Lindsey, FormFactor
Don Locke, LSI Logic
Nick Lycoudes, Motorola
Andy C. Mackie, Ph.D., Praxair Inc.
James F. Maguire, Intel Corporation
Larry May, Alpha Industries
Jeff May, Applied Microcircuit
Dennis McCabe, W. M. Hague
Company
Tom Meuse, Thermo KeyTek
Renee J. Michalkiewicz, Trace
Laboratories - East
Kazutoshi Miyamoto, Mitsubishi
Electric & Electronics
Krishna Mohan, Chartered
Semiconductor
Francois Monette, Cogiscan
Kil-Won Moon, Ph.D., NIST
Gregory C. Munie, Ph.D.
Terry L. Munson, CSL Inc.
Neil Murray, TRW/Automotive
Electronics Group
Graham Naisbitt, Concoat Limited
Larry New, TI
Hon Nguyen, Teradyne
David Nicol
Debora L. Obitz, Trace Laboratories -
East
Gerard A. O'Brien, Photocircuits
Corporation
Richard Onstot, HP
Mario Orduz, Enthone-Polyclad
Technologies
Deepak K. Pai, C.I.D., Advanced
Information Systems
Alan Pan, TwinMos Technologies
Mel Parrish, Soldering Technology
International
James Pau, Conexant Systems
Michael Pavlov, ECI Technology, Inc.
Yeng Peng, Taiwan Semiconductor
Mfg
John Petersen, Microsemi
John W. Porter, Loctite Multicore
Electronics
Siva Prakash, United Test and
Assembly Center
Tapan Pramanik, National
Semiconductor
Andreas Preussger, Infineon
Technologies
Jim D. Raby, Soldering Technology
International
Vicki Reece, Micro Instrument
Jim R. Reed, Dell Computer
Corporation
Nancy W. Reynolds, Kemet
Electronics Corp.
Umberto Ricci, EEMS Italia SpA
Douglas Romm, Texas Instruments
Inc.
Michael M. Rubin, Vishay Sprague
Sanford
William R. Russell, Raytheon
Systems Company
Peter Scala, Hitachi
Angelo Scarcella, EPTAC
Corporation
David F. Scheiner, Kester Northrop
Grumman
Joyce A. Schutt, Sanmina-SCI
Corporation
Rudy Sedlak, RD Chemical Co.
Dr. R. Sengupta, Electronics Regional
Test Lab
William Sepp, Technic Inc.
Robert Sheppard, ASAT
Joseph L. Sherfick, NSWG - Crane
Lowell Sherman, Defense Supply
Center Columbus
Kenneth Sicz, ChipPac
Bill Simmons, Xicor
Tim Skidmore, Raytheon Systems
Company
John E. Sohn Ph.D.
John Solomon, Multisorb
Technologies
David Sorrells, Compaq Computer
Roger Su, L-3 Communications
Simon Su, Advanced Semiconductor
Engineering
Craig Taylor, Actel
Karen A. Tellefsen, Ph.D., Alpha
Metals
Morgan Tench, Ph.D., Rockwell
Science Center
Tracy Tennant, Micron Technology
Ed R. Tidwell, Alcatel USA
Michael Toben, Shipley Ronal
Stephen Todd, FCI Electronics
Brian J. Toleno, Ph.D., Loctite
Corporation
Nick Virmani, Naval Research Lab
W. Lee Vroom, Thomson Consumer
Electronics
Karl F. Wengenroth, Enthone Inc.
George M. Wenger, Celiant
Corporation
Keith J. Whitlaw, Shipley Europe
Ltd.

Maureen Williams, NIST
David Williamson, High Connection
Density
Greg Wood, EMPF/ACI

Thomas A. Woodrow, Ph.D., Boeing
Phantom Works
Shaw Yin, GSI Technology
Michael W. Yuen, Compaq Computer
Corporation

Michael Zampini, Honeywell Canada
Adam R. Zbrzezny, Celestica
International Inc.
Yun Zhang, Ph.D.

John Groom, Transmeta
William Guthrie, IBM
William B. Hampshire, Hampshire
Technical Services
Carol A. Handwerker, Sc.D., NIST
Rodney Hartbauer
Joel Heebink, Honeywell
James D. Herard, IBM Endicott
Electronics Packaging
Steven A. Herrberg, Raytheon
Systems Company
Raif Hijab, T-Ram
David D. Hillman, Rockwell Collins
Phillip E. Hinton, Hinton 'PWB'
Engineering
Andy Hirata, Sharp Microelectronics
Ronald A. Hollandsworth, ITT
Industries
Bruce Houghton, Celestica Inc.
Christopher Hunt, Ph.D., National
Physical Laboratory
Walter Jopke, PolarFab
Lesley M. Kao, Raychem CI &PP
Prakash Kapadia, Celestica
International Inc.
Mario Kasilag, Northrop Grumman
Space Systems
Mark Kelsey, Aspen Research
Corporation
Soo Hyung Kim, Samsung
Electronics
Gregg Klawson, General Dynamics -
C4 Systems
Robert Knoell, Visteon
Tom Kole, Sirenza Microdevices
Jeffry F. Koon, Raytheon Company
Connie M. Korth, Reptron
Manufacturing Services/Hibbing
Mark A. Kwoka, Intersil Corporation
David Lai, Siliconware USA
Leo P. Lambert, EPTAC Corporation
John W. Lampe
Leo LeBlanc, EMC
Frederic W. Lee, Northrop Grumman
Norden Systems
Kuan-Shaur Lei, Compaq Computer
Corporation
David W. LeMay, Silicon Graphics
Computer System
Chou H. Li, LMI Technologies
Boen Li, Photocircuits Corporation
Scott Lindsey, FormFactor
Don Locke, LSI Logic
Nick Lycoudes, Motorola
Andy C. Mackie, Ph.D., Praxair Inc.
James F. Maguire, Intel Corporation
Larry May, Alpha Industries
Jeff May, Applied Microcircuit
Dennis McCabe, W. M. Hague
Company
Jack McCullen, Intel
Tom Meuse, Thermo KeyTek
Renee J. Michalkiewicz, Trace
Laboratories - East
Kazutoshi Miyamoto, Mitsubishi
Electric & Electronics
Krishna Mohan, Chartered
Semiconductor
Francois Monette, Cogiscan
Kil-Won Moon, Ph.D., NIST
Gregory C. Munie, Ph.D.
Terry L. Munson, CSL Inc.
Neil Murray, TRW/Automotive
Electronics Group
Graham Naisbitt, Concoat Limited
Larry New, TI
Hon Nguyen, Teradyne
David Nicol
Debora L. Obitz, Trace Laboratories -
East
Gerard A. O'Brien, Photocircuits
Corporation
Richard Onstot, HP
Mario Orduz, Enthone-Polyclad
Technologies
Deepak K. Pai, C.I.D., Advanced
Information Systems
Alan Pan, TwinMos Technologies
Mel Parrish, Soldering Technology
International
James Pau, Conexant Systems
Michael Pavlov, ECI Technology, Inc.
Yeng Peng, Taiwan Semiconductor
Mfg
John Petersen, Microsemi
John W. Porter, Loctite Multicore
Electronics
Siva Prakash, United Test and
Assembly Center
Tapan Pramanik, National
Semiconductor
Andreas Preussger, Infineon
Technologies
Jim D. Raby, Soldering Technology
International
Vicki Reece, Micro Instrument
Jim R. Reed, Dell Computer
Corporation
Nancy W. Reynolds, Kemet
Electronics Corp.
Umberto Ricci, EEMS Italia SpA
Douglas Romm, Texas Instruments
Inc.
Michael M. Rubin, Vishay Sprague
Sanford
William R. Russell, Raytheon
Systems Company
Peter Scala, Hitachi
Angelo Scarcella, EPTAC
Corporation
David F. Scheiner, Kester Northrop
Grumman
Joyce A. Schutt, Sanmina-SCI
Corporation
Rudy Sedlak, RD Chemical Co.
Dr. R. Sengupta, Electronics Regional
Test Lab
William Sepp, Technic Inc.
Robert Sheppard, ASAT
Joseph L. Sherfick, NSWC - Crane
Lowell Sherman, Defense Supply
Center Columbus
Kenneth Sicz, ChipPac
Bill Simmons, Xicor
Tim Skidmore, Raytheon Systems
Company
John E. Sohn Ph.D.
John Solomon, Multisorb
Technologies
David Sorrells, Compaq Computer
Roger Su, L-3 Communications
Simon Su, Advanced Semiconductor
Engineering
Craig Taylor, Actel
Karen A. Tellefsen, Ph.D., Alpha
Metals
Morgan Tench, Ph.D., Rockwell
Science Center
Tracy Tennant, Micron Technology
Ed R. Tidwell, Alcatel USA
Michael Toben, Shipley Ronal
Stephen Todd, FCI Electronics
Brian J. Toleno, Ph.D., Loctite
Corporation
Nick Virmani, Naval Research Lab
W. Lee Vroom, Thomson Consumer
Electronics
Karl F. Wengenroth, Enthone Inc.
George M. Wenger, Celiant
Corporation

Keith J. Whitlaw, Shipley Europe
Ltd.

Maureen Williams, NIST

David Williamson, High Connection
Density

Greg Wood, EMPF/ACI

Thomas A. Woodrow, Ph.D., Boeing
Phantom Works

Shaw Yin, GSI Technology

Michael W. Yuen, Compaq Computer
Corporation

Michael Zampini, Honeywell Canada

Adam R. Zbrzezny, Celestica
International Inc.

Yun Zhang, Ph.D.

MOISTURE/REFLOW SENSITIVITY CLASSIFICATION FOR NONHERMETIC SOLID STATE SURFACE MOUNT DEVICES

1 PURPOSE

The purpose of this standard is to identify the classification level of non-hermetic solid state surface mount devices (SMDs) that are sensitive to moisture-induced stress so that they can be properly packaged, stored, and handled to avoid damage during assembly solder reflow attachment and/or repair operations.

This standard may be used to determine what classification/preconditioning level should be used for SMD package qualification. Passing the criteria in this test method is not sufficient by itself to provide assurance of long-term reliability.

1.1 Scope This classification procedure applies to all non-hermetic solid state Surface Mount Devices (SMDs) in packages, which, because of absorbed moisture, could be sensitive to damage during solder reflow. The term SMD as used in this document means plastic encapsulated surface mount packages and other packages made with moisture-permeable materials. The categories are intended to be used by SMD producers to inform users (board assembly operations) of the level of moisture sensitivity of their product devices, and by board assembly operations to ensure that proper handling precautions are applied to moisture/reflow sensitive devices. If no major changes have been made to a previously qualified SMD package, this method may be used for reclassification according to 4.1.

This standard cannot address all of the possible component, board assembly and product design combinations. However, the standard does provide a test method and criteria for commonly used technologies. Where uncommon or specialized components or technologies are necessary, the development should include customer/manufacture involvement and the criteria should include an agreed definition of product acceptance.

SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak reflow temperature is desired.

Note: If the procedures in this document are used on packaged devices that are not included in this specification's scope, the failure criteria for such packages must be agreed upon by the device supplier and their end user.

1.2 Background The vapor pressure of moisture inside a non-hermetic package increases greatly when the package is exposed to the high temperature of solder reflow. Under certain conditions, this pressure can cause internal delamination of the packaging materials from the die and/or leadframe/substrate, internal cracks that do not extend to the outside of the package, bond damage, wire necking, bond lifting, die lifting, thin film cracking, or cratering beneath the bonds. In the most severe case, the stress can result in external package cracks. This is commonly referred to as the "popcorn" phenomenon because the internal stress causes the package to bulge and then crack with an audible "pop." SMDs are more susceptible to this problem than through-hole parts because they are exposed to higher temperatures during reflow soldering. The reason for this is that the soldering operation must occur on the same side of the board as the SMD device. For through-hole devices, the soldering operation occurs under the board that shields the devices from the hot solder.

2 APPLICABLE DOCUMENTS

2.1 Electronic Industries Alliance (EIA-JEDEC)¹

JESD22-A120 Test Method for the Measurement of Moisture Diffusivity and Water Solubility in Organic Materials Used in Integrated Circuits

JESD22-A113 Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing

JESD 47 Stress Test Driven Qualification Specification

JESD-625 Requirements for Handling Electrostatic Discharge Sensitive (ESD) Devices

1. www.jedec.org

2.2 IPC²

IPC-TM-650 Test Methods Manual³

2.1.1 Microsectioning

2.1.1.2 Microsectioning - Semi or Automatic Technique Microsection Equipment

2.3 Joint Industry Standards⁴

J-STD-033 Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

J-STD-035 Acoustic Microscopy for Non-hermetic Encapsulated Electronic Components

3 APPARATUS

3.1 Temperature Humidity Chambers Moisture chamber(s), capable of operating at 85°C/85% RH, 85°C/60% RH, 60°C/60% RH, and 30°C/60% RH. Within the chamber working area, temperature tolerance must be $\pm 2^\circ\text{C}$ and the RH tolerance must be $\pm 3\%$ RH.

3.2 Solder Reflow Equipment

3.2.1 Full Convection (Preferred) Full convection reflow system capable of maintaining the reflow profiles required by this standard.

3.2.2 Infrared Infrared (IR)/convection solder reflow equipment capable of maintaining the reflow profiles required by this standard. It is required that this equipment use IR to heat only the air and not directly impinge upon the SMD Packages/devices under test.

Note: The moisture sensitivity classification test results are dependent upon the package body temperature (rather than the mounting substrate and/or package terminal temperature).

3.3 Ovens Bake oven capable of operating at 125 $\pm 5/0^\circ\text{C}$.

3.4 Microscopes

3.4.1 Optical Microscope Optical Microscope (40X for external and 100X for cross-section exam).

3.4.2 Scanning Acoustic Microscope Scanning acoustic microscope with C-Mode and Through Transmission capability and capable of measuring a minimum delamination of 5% of the area being evaluated.

Note 1: The scanning acoustic microscope is used to detect cracking and delamination. However, the presence of delamination does not necessarily indicate a pending reliability problem. The reliability impact of delamination must be established for a particular die/package system.

Note 2: Refer to IPC/JEDEC J-STD-035 for operation of the scanning acoustic microscope.

3.5 Cross-Sectioning Micro-sectioning equipment as recommended per IPC-TM-650 Methods 2.1.1, 2.1.1.2 or other applicable document.

3.6 Electrical Test Electrical test equipment with capabilities to perform appropriate testing on devices.

3.7 Weighing Apparatus (Optional) Weighing apparatus capable of weighing the package to a resolution of 1 microgram. This apparatus must be maintained in a draft-free environment, such as a cabinet. It is used to obtain absorption and desorption data on the devices under test (see Clause 8).

2. www.ipc.org

3. Current and revised IPC Test Methods are available through IPC-TM-650 subscription and on the IPC Web site (www.ipc.org/html/testmethods.htm).

4. www.jedec.org / www.ipc.org

4 CLASSIFICATION/RECLASSIFICATION

Refer to 4.1 for guidance on reclassification of previously qualified/classified SMDs.

Engineering studies have shown that thin, low volume SMD packages reach higher body temperatures during reflow soldering to boards that have been profiled for larger packages. Therefore, technical and/or business issues normally require thin, low volume SMD packages (reference Table 4-1) to be classified at higher reflow temperatures.

Note 1: Previously classified SMDs should only be reclassified by the manufacturer. Users should refer to the “Moisture Sensitivity” label on the bag to determine at which reflow temperature the SMD packages were classified.

Note 2: Level 1 SMD packages should be considered to have a maximum reflow temperature of 220°C unless labeled as capable of reflow at other temperatures.

Table 4-1 Package Peak Reflow Temperatures

Reflow Conditions	Pkg. Thickness ≥ 2.5 mm or Pkg. Volume ≥ 350 mm ³	Pkg. Thickness < 2.5 mm and Pkg. Volume < 350 mm ³
SnPb Eutectic	Convection 225 +0/-5°C	Convection 245 +0/-5°C
Pb Free	Convection 240 +0/-5°C	Convection 250 +0/-5°C

Note 1: Package volume excludes external terminals (balls, bumps, lands, leads) and or non-integral heat sinks.

Note 2: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Note 3: Components intended for use in a “lead-free” assembly process shall be evaluated using the “lead free” peak temperature and profiles defined in Tables 4-1 and 5-2 whether or not lead free.

Note 4: It is possible that very large (≥ 45 cm X 60 cm) thick (≥ 3 mm) boards that use components with a wide range of thermal mass might have difficulty maintaining all component bodies below the maximum temperatures in this specification. In such cases, the user and/or supplier must determine the MSL level at the body temperature the component is actually exposed to.

4.1 Reclassification SMD packages previously classified to a moisture sensitivity level and reflow peak temperature may be reclassified if the damage response (delamination/cracking) at the more severe condition for items listed in 6.1 and 6.2 is less than, or equal to the damage response at the original classification condition.

If no major changes have been made to a previously qualified SMD package, this method may be used for reclassification to an improved level (longer floor life) at the same reflow temperature. The reclassification level cannot be improved by more than one level without additional reliability testing. Reclassification to level 1 requires additional reliability testing.

If no major changes have been made to a previously qualified SMD package, this method may be used for reclassification at a higher reflow temperature providing the moisture level remains the same or degrades to a more sensitive level.

No SMD packages classified as moisture sensitive by any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) may be reclassified as non-moisture sensitive (level 1) without additional reliability stress testing, e.g., JESD22-A113 and JESD47 or the semiconductor manufacturer’s in-house procedures.

To minimize testing, the results from a given SMD package may be generically accepted to cover all other devices which are manufactured in the same package, using the same packaging materials (die attach, mold compound and or die coating, etc.), with the die using the same wafer fabrication technology, and with die pad dimensions not greater than those qualified.

The following attributes could affect the moisture sensitivity of a device and may require reclassification:

- Die attach material/process
- Number of pins
- Encapsulation (Mold compound or Glob Top) material/process
- Die pad area and shape
- Body size
- Passivation/die coating
- Leadframe, substrate, and/or heat spreader design/material/finish
- Die size/thickness
- Wafer Fabrication technology/process
- Interconnect
- Lead lock taping size/location as well as material

5 PROCEDURE

The recommended procedure is to start testing at the lowest moisture sensitivity level the evaluation package is reasonably expected to pass (based on knowledge of other similar evaluation packages).

In the case of equipment malfunction, operator error or electrical power loss, engineering judgment shall be used to ensure that the minimum intent/requirements of this specification are met.

5.1 Sample Requirements

5.1.1 Reclassification (qualified package without additional reliability testing) For a qualified SMD package being reclassified without additional reliability testing select a minimum sample of 22 units for each moisture sensitivity level to be tested. A minimum of two nonconsecutive assembly lots must be included in the sample with each lot having approximately the same representation. Sample units shall have completed all manufacturing processing required prior to shipment. Sample groups may be run concurrently on one or more moisture sensitivity levels.

5.1.2 Classification/Reclassification Select a minimum sample of 11 units for each moisture sensitivity level to be tested. A minimum of two nonconsecutive assembly lots must be included in the sample with each lot having approximately the same representation. Sample units shall have completed all manufacturing processes required prior to shipment. Sample groups may be run concurrently on one or more moisture sensitivity levels. Testing must be continued until a passing level is found.

SMD packages should not be reclassified by the user unless approved by the supplier.

5.2 Initial Electrical Test Test appropriate electrical parameters, e.g., data sheet values, in house specifications, etc. Replace any components, while maintaining the sample requirements of 5.1.2, which fail to meet tested parameters.

5.3 Initial Inspection Perform an external visual and acoustic microscope examination, on all components, to establish a baseline for the cracking/delamination criteria in 6.2.1.

Note: This standard does not consider or establish any accept/reject criteria for delamination at initial/time zero inspection.

5.4 Bake Bake the sample for 24 hours minimum at 125 \pm 5/-0°C. This step is intended to remove moisture from the package so that it will be “dry.”

Note: This time/temperature may be modified if desorption data on the particular device under test shows that a different condition is required to obtain a “dry” package when starting in the wet condition for 85°C/85% RH. See 8.3.

5.5 Moisture Soak Place devices in a clean, dry, shallow container so that the package bodies do not touch or overlap each other. Submit each sample to the appropriate soak requirements shown in Table 5-1. At all times parts should be handled using proper ESD procedures in accordance with JESD 625.

5.6 Reflow Not sooner than 15 minutes and not longer than 4 hours after removal from the temperature/humidity chamber, subject the sample to 3 cycles of the appropriate reflow conditions as defined in Table 5-2 and Figure 5-1. If the timing between removal from the temperature/humidity chamber and initial reflow cannot be met then the parts must be rebaked and resoaked according to 5.4 and 5.5. The time between reflows shall be 5 minutes minimum and 60 minutes maximum.

5.7 Final External Visual Examine the devices using an optical microscope (40X) to look for external cracks.

5.8 Final Electrical Test Perform appropriate electrical testing on all devices, e.g., data sheet values, in-house specifications, etc.

5.9 Final Acoustic Microscopy Perform scanning acoustic microscope analysis on all devices.

**Table 5-1
Moisture Sensitivity Levels**

LEVEL	FLOOR LIFE		SOAK REQUIREMENTS			
			STANDARD		ACCELERATED EQUIVALENT ¹	
	TIME	CONDITIONS	TIME (hours)	CONDITIONS	TIME (hours)	CONDITIONS
1	Unlimited	≤30°C/85% RH	168 +5/-0	85°C/85% RH		
2	1 year	≤30°C/60% RH	168 +5/-0	85°C/60% RH		
2a	4 weeks	≤30°C/60% RH	696 ² +5/-0	30°C/60% RH	120 +1/-0	60°C/60% RH
3	168 hours	≤30°C/60% RH	192 ² +5/-0	30°C/60% RH	40 +1/-0	60°C/60% RH
4	72 hours	≤30°C/60% RH	96 ² +2/-0	30°C/60% RH	20 +0.5/-0	60°C/60% RH
5	48 hours	≤30°C/60% RH	72 ² +2/-0	30°C/60% RH	15 +0.5/-0	60°C/60% RH
5a	24 hours	≤30°C/60% RH	48 ² +2/-0	30°C/60% RH	10 +0.5/-0	60°C/60% RH
6	Time on Label (TOL)	≤30°C/60% RH	TOL	30°C/60% RH		

Note 1: CAUTION – The “accelerated equivalent” soak requirements shall not be used until correlation of damage response, including electrical, after soak and reflow is established with the “standard” soak requirements or if the known activation energy for diffusion is 0.4 - 0.48 eV. Accelerated soak times may vary due to material properties, e.g., mold compound, encapsulant, etc. JEDEC document JESD22-120 provides a method for determining the diffusion coefficient.

Note 2: The standard soak time includes a default value of 24 hours for semiconductor manufacturer’s exposure time (MET) between bake and bag and includes the maximum time allowed out of the bag at the distributor’s facility.

If the actual MET is less than 24 hours the soak time may be reduced. For soak conditions of 30°C/60% RH the soak time is reduced by 1 hour for each hour the MET is less than 24 hours. For soak conditions of 60°C/60% RH, the soak time is reduced by 1 hour for each 5 hours the MET is less than 24 hours.

If the actual MET is greater than 24 hours the soak time must be increased. If soak conditions are 30°C/60% RH, the soak time is increased 1 hour for each hour that the actual MET exceeds 24 hours. If soak conditions are 60°C/60% RH, the soak time is increased 1 hour for each 5 hours that the actual MET exceeds 24 hours.

Note 3: Supplier may extend the soak times at their own risk.

Table 5-2 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly		Pb-Free Assembly	
	Large Body	Small Body	Large Body	Small Body
Average ramp-up rate (T _L to T _p)	3°C/second max.		3°C/second max.	
Preheat				
– Temperature Min (T _{smin})	100°C		150°C	
– Temperature Max (T _{smax})	150°C		200°C	
– Time (min to max) (ts)	60-120 seconds		60-180 seconds	
T _{smax} to T _L				
– Ramp-up Rate			3°C/second max	
Time maintained above:				
– Temperature (T _L)	183°C		217°C	
– Time (t _L)	60-150 seconds		60-150 seconds	
Peak Temperature (T _p)	225 +0/-5°C	240 +0/-5°C	245 +0/-5°C	250 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.		6°C/second max.	
Time 25°C to Peak Temperature	6 minutes max.		8 minutes max.	

Note: All temperatures refer to topside of the package, measured on the package body surface.

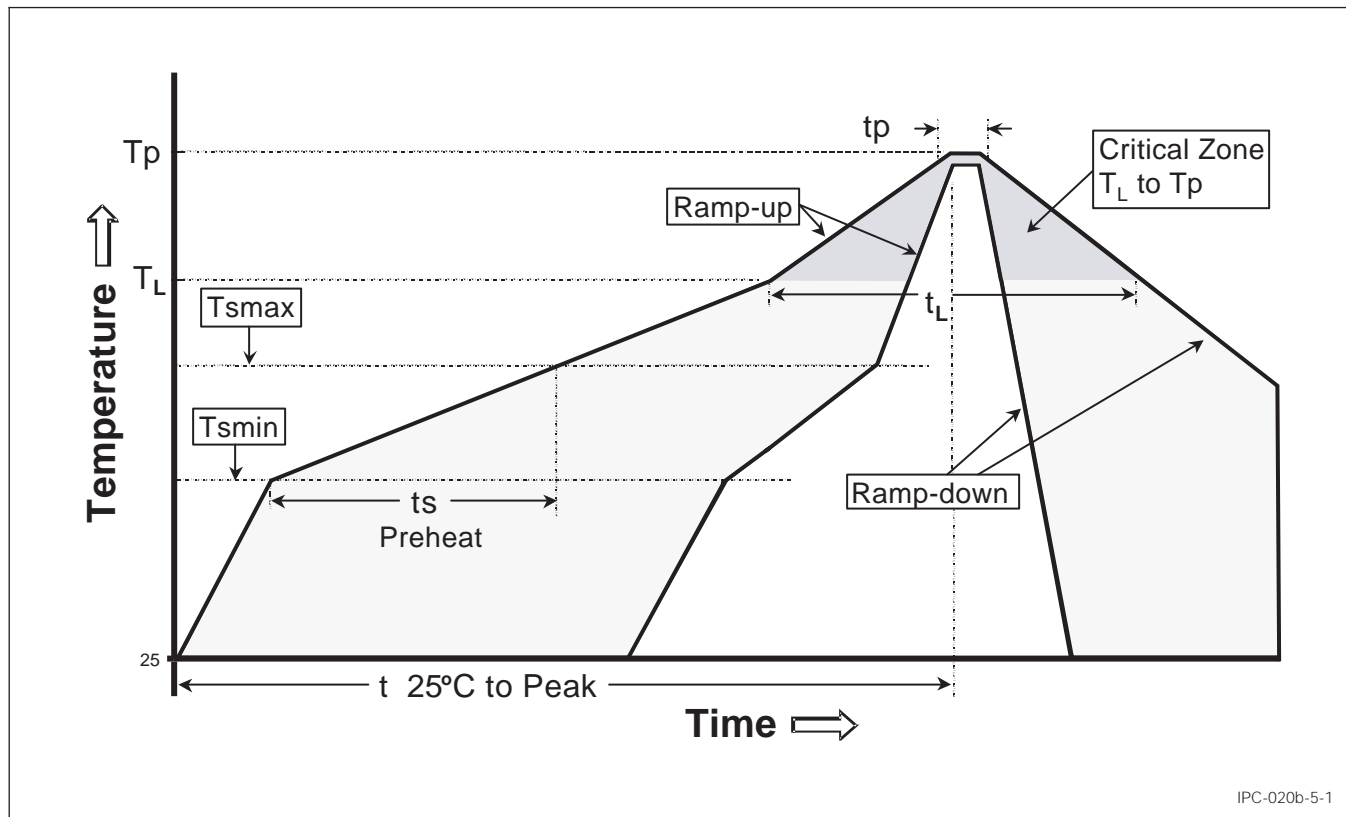


Figure 5-1 Classification Reflow Profile

6 CRITERIA

6.1 Failure Criteria If one or more devices in the test sample fail, the package shall be considered to have failed the tested level.

A device is considered a failure if it exhibits any of the following:

- External crack visible using 40X optical microscope
- Electrical test failure
- Internal crack that intersects a bond wire, ball bond, or wedge bond
- Internal crack extending from any lead finger to any other internal feature (lead finger, chip, die attach paddle)
- Internal crack extending more than two-thirds (2/3) the distance from any internal feature to the outside of the package
- Changes in package body flatness caused by warpage, swelling or bulging visible to the naked eye. If parts still meet co-planarity and standoff dimensions they shall be considered passing.

Note 1: If internal cracks are indicated by acoustic microscopy, they must be considered a failure or verified good using polished cross sections through the identified site.

Note 2: For packages known to be sensitive to vertical cracks it is recommended that polished cross sections be used to confirm the non-existence of near vertical cracks within the mold compound or encapsulant.

Note 3: Failing SMD packages must be evaluated to a higher numeric level of moisture sensitivity using a new set of samples.

Note 4: If the components pass the requirements of 6.1, and there is no evidence of delamination or cracks observed by acoustic microscopy or other means, the component is considered to pass that level of moisture sensitivity.

6.2 Criteria Requiring Further Evaluation To evaluate the impact of delamination on device reliability, the semiconductor manufacturer may either meet the delamination requirements shown in 6.2.1 or perform reliability assessment using JESD22-A113 and JESD47 or the semiconductor manufacturer's in-house procedures. The reliability assessment may consist of stress testing, historical generic data analysis, etc. Annex A shows the logic flow diagram for the implementation of these criteria.

If the SMD Packages pass electrical tests and there is delamination on the back side of the die paddle, heat spreader, die back side (lead on chip only) but there is no evidence of cracking, or other delamination, and they still meet specified dimensional criteria, the SMD Packages are considered to pass that level of moisture sensitivity.

6.2.1 Delamination The following delamination changes are measured from pre-moisture soak to post reflow. A delamination change is the change between pre- and post-reflow. The percent (%) delamination change is calculated in relation to the total area being evaluated.

6.2.1.1 Metal Leadframe Packages:

- a. No delamination on the active side of the die.
- b. No delamination change >10% on any wire bonding surface of the die paddle (downbond area) or the leadframe of LOC (Lead On Chip) devices.
- c. No delamination change >10% along any polymeric film bridging any metallic features that is designed to be isolated (verifiable by through transmission acoustic microscopy).
- d. No delamination/cracking change >10% through the die attach region in thermally enhanced packages or devices that require electrical contact to the backside of the die.
- e. No surface-breaking feature delaminated over its entire length. A surface-breaking feature includes: lead fingers, tie bars, heat spreader alignment features, heat slugs, etc.

6.2.1.2 Substrate Based Packages (e.g. BGA, LGA etc.):

- a. No delamination on the active side of the die
- b. No delamination change >10% on any wire bonding surface of the laminate
- c. No delamination change >10% along the polymer potting or molding compound/laminate interface for cavity and over-molded packages
- d. No delamination change >10% along the solder mask/laminate resin interface
- e. No delamination change >10% within the laminate
- f. No delamination/cracking change >10% through the die attach region
- g. No delamination/cracking between underfill resin and chip or underfill resin and substrate/solder mask.
- h. No surface-breaking feature delaminated over its entire length. A surface-breaking feature includes lead fingers, laminate, laminate metallization, PTH, heat slugs, etc.

Note: On substrate based packages, the C-mode acoustic image is not easy to interpret. Through transmission acoustic imaging is recommended because it is easier to interpret and more reliable. If it is necessary to verify results or determine at what level in the package the cracking/delamination is occurring, cross-sectional analysis should be used.

6.3 FAILURE VERIFICATION All failures should be analyzed to confirm that the failure mechanism is associated with moisture sensitivity. If there are no reflow moisture-sensitive-induced failures in the level selected, the component meets the tested level of moisture sensitivity.

If the acoustic microscope scans show failure to any of the criteria listed in 6.2.1, the SMD Packages shall be tested to a higher numeric level of moisture sensitivity or subjected to a reliability assessment using JESD22-A113 and JESD47 or the semiconductor manufacturer's in-house procedures.

7 MOISTURE/REFLOW SENSITIVITY CLASSIFICATION

If a device passes level 1, it is classified as not moisture sensitive and does not require dry pack.

If a device fails level 1 but passes a higher numerical level, it is classified as moisture sensitive and must be dry packed in accordance with J-STD-033.

If a device will only pass level 6, it is classified as extremely moisture sensitive and dry pack will not provide adequate protection. If this product is shipped, the customer must be advised of its classification. The supplier must also include a warning label with the device indicating that it either be socket mounted, or baked dry within time on label before reflow soldering. The minimum bake time and temperature should be determined from desorption studies of the device under test. See 8.3.

8 OPTIONAL WEIGHT GAIN/LOSS ANALYSIS

8.1 Weight Gain Weight gain analysis (absorption) can be very valuable in determining estimated floor life (the time from removal of a device from dry pack until it absorbs sufficient moisture to be at risk during reflow soldering). Weight loss analysis (desorption) is valuable in determining the bake time required to remove excess moisture from a device so that it will no longer be at risk during reflow soldering. Weight gain/loss is calculated using an average for the entire sample. It is recommended that ten (10) devices be used in the sample.

Final weight gain = (wet weight - dry weight)/dry weight.

Final weight loss = (wet weight - dry weight)/wet weight.

Interim weight gain = (present weight - dry weight)/dry weight.

Interim weight loss = (wet weight - present weight)/wet weight

“Wet” is relative and means the package is exposed to moisture under specific temperature and humidity conditions.

“Dry” is specific and means no additional moisture can be removed from the package at 125°C.

8.2 Absorption Curve

8.2.1 Read Points The X-axis (time) read points should be selected for plotting the absorption curve. For the early readings, points should be relatively short (24 hours or less) because the curve will have a steep initial slope. Later readings may be spread out further (10 days or more) as the curve becomes asymptotic. The Y-axis (weight gain) should start with “0” and increase to the saturated weight gain. Most devices will reach saturation between 0.3% and 0.4% when stored at 85 °C/85% RH. Use the formula in 8.1. Devices shall be kept at room ambient between removal from the oven or chamber and weighing and subsequent reinsertion into the oven or chamber.

8.2.2 Dry Weight The dry weight of the sample should be determined first. Bake the sample for 48 hours minimum at 125 +5/-0 °C to ensure that the devices are dry. Within one (1) hour after removal from the oven, weigh the devices using the optional equipment in 3.7 and determine an average dry weight per 8.1. For small SMDs (less than 1.5 mm total height), devices should be weighed within thirty (30) minutes after removal from oven.

8.2.3 Moisture Soak Within one (1) hour after weighing, place the devices in a clean, dry, shallow container so that the package bodies do not touch each other. Place the devices in the desired temperature/humidity condition for the desired length of time.

8.2.4 Readouts Upon removal of the devices from the temperature/humidity chamber, allow devices to cool for at least 15 minutes. Within one (1) hour after removal from the chamber, weigh the devices. For small SMDs (less than 1.5 mm total height), devices should be weighed within thirty (30) minutes after removal from the chamber. After the devices are weighed, follow the procedure in 8.2.3 for placing the devices back in the temperature/humidity chamber. No more than two (2) hours total time should elapse between removal of devices from the temperature/humidity chamber and their return to the chamber.

Continue alternating between 8.2.3 and 8.2.4 until the devices reach saturation as indicated by no additional increase in moisture absorption or until soaked to the maximum time of interest.

8.3 Desorption Curve A desorption curve can be plotted using devices that have reached saturation as determined in 8.2.

8.3.1 Read Points The suggested read points on the X-axis are 12 hour intervals. The Y-axis should run from “0” weight gain to the saturated value as determined in 8.2.

8.3.2 Baking Within one (1) hour (but not sooner than fifteen (15) minutes) after removal of the saturated devices from the temperature/humidity chamber, place the devices in a clean, dry, shallow container so that the package bodies do not touch each other. Place the devices in the bake oven at the desired temperature for the desired time.

8.3.3 Readouts At the desired read point; remove the devices from the bake oven. Within one (1) hour after removal of the devices from the bake oven, remove the devices from the container and determine their average weight using the optional equipment in 3.7 and formula in 8.1.

Within one (1) hour after weighing the devices, place them in a clean, dry, shallow container so that the package bodies do not touch each other. Return the devices to the bake oven for the desired time.

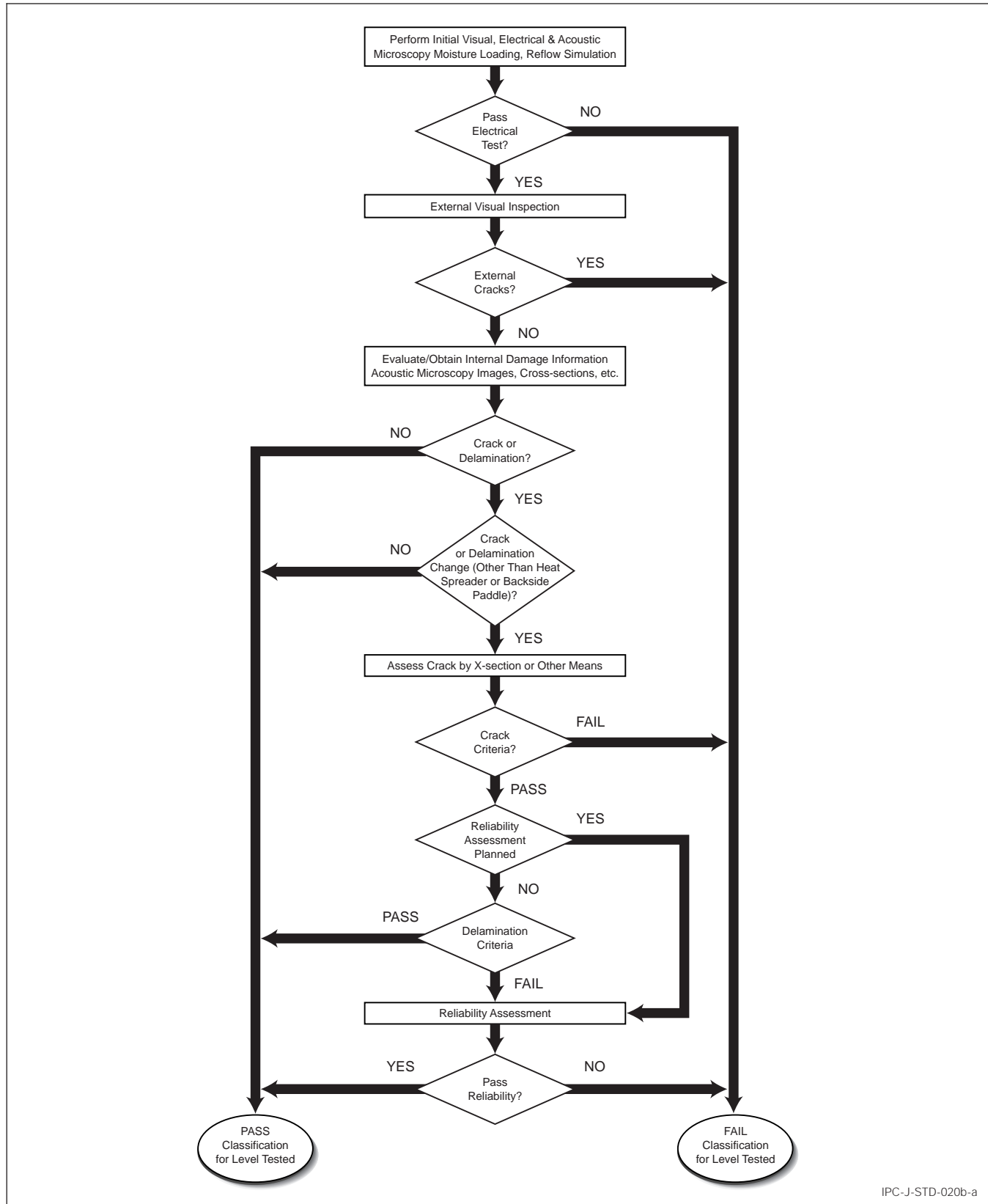
Continue until the devices have lost all their moisture as determined by the dry weight in 8.2.2.

11 ADDITIONS AND EXCEPTIONS

The following details shall be specified in the applicable procurement document:

- a. Device selection criteria if different from 5.1.
- b. Test procedure sample size if different from 5.1.
- c. Package types to be evaluated.
- d. Any reject criteria (including Scanning Acoustic Microscope criterion) in addition to those shown in Clause 6.
- e. Any preconditioning requirements beyond those shown in Clause 5.
- f. Conditions or frequency under which retest is required.

Annex A Classification Flow





ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES

Standard Improvement Form

IPC/JEDEC J-STD-020B

The purpose of this form is to provide the Technical Committee of IPC with input from the industry regarding usage of the subject standard.

Individuals or companies are invited to submit comments to IPC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

IPC
2215 Sanders Road
Northbrook, IL 60062-6135
Fax 847 509.9798

1. I recommend changes to the following:

Requirement, paragraph number _____
 Test Method number _____, paragraph number _____

The referenced paragraph number has proven to be:

Unclear Too Rigid In Error
 Other _____

2. Recommendations for correction:

3. Other suggestions for document improvement:

Submitted by:

Name

Telephone

Company

E-mail

Address

City/State/Zip

Date



ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES

ISBN #1-580987-03-6

2215 Sanders Road, Northbrook, IL 60062-6135
Tel. 847.509.9700 Fax 847.509.9798
www.ipc.org